REMARKS

This responds to the Office Action mailed on February 13, 2008.

Claims 1-3, 6, 9, 10 and 12 are amended, no claims are canceled, and claims 13-20 are added; thus, claims 1-20 remain pending in this application.

Claim Objections

Claims 1, 2, 3, 6, and 9-10 were objected to because of informalities. Applicant has amended claims 1, 2, 3, 6 and 9-10 and respectfully requests reconsideration and withdrawal of the objections.

Information Disclosure Statement

Applicant resubmits the Lakhani (Serial Number: 09/223,087) reference for consideration.

Double Patenting Rejection

Claims 1-4 and 6-12 were rejected on the ground of non-statutory obviousness-type double patenting as being unpatentable over claims 11, 14, 15 and 18-21 of U.S. Patent No.6,601,191.

Applicant acknowledges the rejection and will respond appropriately when the claims of the present application are otherwise found allowable.

§112 Rejection of the Claims

Claims 1, 2 and 9-12 were rejected under 35 U.S.C. § 112, second paragraph.

Claims 4-5 and 7-8 were also rejected because they depend on a base rejected claim and have the same problems for insufficient antecedent basis.

Applicant has amended the claims to further clarify the recited subject matter and respectfully requests withdrawal of the rejections, and reconsideration and allowance of claims 1, 2, 4-5 and 7-12.

§102 Rejection of the Claims

Claims 1-12 were rejected under 35 U.S.C. § 102(e) for anticipation by Endoh et al. (Endoh) (U.S 5,602,789). Applicant does not admit Endoh is prior art and reserves the right to swear behind the reference, however, Applicant has chosen to distinguish the claims from the reference. Applicant respectfully traverses the rejection for at least the following reasons.

Insofar as the rejection is applied to claims 1, 3, 6 and 9, the rejection relies on FIG.7 of Endoh. Endoh describes the circuit of FIG. 7 as a "word line controller" (Endoh, col. 13, lines 45-50). The specification of Endoh further describes the circuit of FIG. 7 as including five voltage generating circuits connected to word line WLj (Endoh, col. 13, lines 50-55), where some of the voltages may be used for controlling the word line for write verification purposes. Also, word line, WLj, is the only output of the word line controller circuit of FIG. 7. Endoh describes the word line controller as responding to control signals to apply one of the voltages of the circuit to word lines for programming, including erasing, and reading stored information from the memory array (Endoh, col. 13 line 54 to col. 14 line 3). However, Applicant submits the circuit of FIG. 7 does not teach, show or suggest an over programming condition detector. The rejection also recites that the Endoh reference shows a fourth logic gate (Endoh, FIG. 7, 110B) for receiving data written to the array (Office Action, pg. 14). Applicant is unable to find in FIG. 7, or the cited portions of the Endoh specifications, where the 110B circuit of FIG. 7 receives data written to the array. Therefore, for the reasons above, Applicant submits the gates referenced in Endoh by the rejection as detectors of an over-programming condition (pgs. 14-18) merely connect one of the reference voltages of the FIG. 7 circuit to word line, WLj, in response to a command signal.

Claims 1, 3, 6 and 9 also recite a device, over-programming condition detector or system comprising or for use with an array of multistate memory cells, "each cell programmable to store an amount of electric charge representative of a desired state selected from at least four sequential data states". Applicant submits the cited portions of Endoh relate to an circuit responsive to command signals for writing, write verifying, reading, erasing and erase verifying memory cells, however a command signal does not indicate the amount of charge programmed

into a cell to represent one of at least four sequential data states capable of being programmed in the cell. Thus the command signal does not indicate that the cell is over-programmed.

The rejection asserts that the control circuit 110B, FIG. 7 of Endoh anticipates "a first logic gate for detecting a first one of the sequential data states in the data intended to be written to the array" as recited in claims 1, 3 and 6. However, the control circuit 110B of Endoh, FIG. 7, is shown and described as applying a ground type voltage to word line WLj when the circuit responds to a command signal such as ERASE, E-VERIFY or, a READ command signal associated with address line a_i.

The rejection asserts that the circuit 106 of Endoh FIG. 7, anticipates "a second gate for detecting a second one of the sequential data states in data intended to be written to the array" as recited in claims 1, 3 and 6. However, the circuit 106 of Edoh FIG. 7 is shown and described as applying a voltage, Vver1, to word line WLj in response to a W-VERIFY1 command signal associated with address line a_i .

The rejection asserts that the circuit 108 of Endoh, FIG. 7, anticipates " a third logic gate for detecting a third one of the sequential data states in data intended to be written to the array" as recited in claims 1, 3 and 6. However, circuit 108 of Endoh, FIG. 7 is clearly shown and further described as applying a voltage, Vver2, to word line WLj in response to a W-VERIFY2 command signal associated with address line a_i .

The rejection asserts that the control circuit 110B, FIG. 7 of Endoh anticipates "a fourth logic gate for receiving data written to the array" as recited in claims 1, 3 and 6. However, the control circuit 110B of Endoh, FIG. 7, is shown and described as applying a ground type voltage to word line WLj when the circuit responds to a command signal such as ERASE, E-VERIFY or a READ command signal assciated with address line a_i. Additionally, as noted above, Applicant is unable to find where the cited circuit receives the data written to the array as the inputs to circuit 110B appear to include command signals and address lines.

In summary, Applicant submits at least circuits 110B, 106 and 108 of Endoh, FIG. 7 do not detect data states of data intended to be written to an array and further reiterates that the circuit of Endoh, FIG. 7, is not a over-programming detector but a write line and write verification controller.

Claims 1 and 2

For the reasons provided above, with respect to claim 1, Applicant is unable to find, among other things, in the cited portions of Endoh, an over-programming condition detector for use with an array of multistate memory cells comprising a first logic gate, a second logic gate, a third logic gate, a fourth logic gate for receiving data written to the array, and over-programming detection logic connected to the first, second, third and fourth logic gates for generating an over-programming condition signal. Applicant respectfully request the withdrawal of the rejection, and reconsideration and allowance of claim 1.

Claim 2 depend on independent claim 1 and is believed to be in a condition for allowance at least for the reasons provided for claim 1.

Claims 3-5

With respect to claim 3, in addition to the above reasons, Applicant believes the rejection mischaracterizes the cited portions of the Endoh associated with the fourth, fifth and sixth logic gates as detectors. Endoh provides, through the description of FIG. 7, that Nodes N2, N3 and N4 of word line WLj will assume the various voltages supplied to the circuit when logic circuits 102, 104, 106, 108, 110A and 110B respond to command signals for controlling wordline WLj. In other words, under normal conditions, nodes N2, N3 and N4 will assume predictable, predetermined voltage levels, corresponding to the voltage level commanded and not dependent on whether the memory cell accessed is over-programmed. Therefore, Applicant is unable to find, among other things, in the cited portions of Endoh, an over-programming condition detector comprising a first gate logic gate, a second logic gate, a third logic gate, a fourth logic gate for detecting a first over-programmed condition, a fifth logic gate for detecting a second over-programmed condition and a sixth logic gate for detecting a third over-programmed condition as recited in claim 3. Applicant respectfully request the withdrawal of the rejection, and reconsideration and allowance of claim 3.

Claims 4 and 5 depend, either directly or indirectly, on independent claim 3 and are believed to be in condition for allowance at least for the reasons provided with respect to independent claim 3.

Claims 6-8

With respect to claim 6, in addition to the above reasons, Applicant believes the rejection mischaracterizes the cited portions of the Endoh associated with the fourth, fifth and sixth logic gates as detectors. Endoh provides, through the description of FIG. 7, that Nodes N2, N3 and N4 of word line, WLj, will assume the various voltages supplied to the circuit when logic circuits 102, 104, 106, 108, 110A and 110B respond to command signals for controlling word line, WLj. In other words, under normal conditions, nodes N2, N3 and N4 will assume predictable, predetermined voltage levels, corresponding to the voltage level commanded and not dependent on whether the memory cell accessed is over-programmed. Therefore, Applicant is unable to find, among other things, in the cited portions of Endoh, an over-programming condition detector comprising a first logic gate, a second logic gate, a third logic gate, a fourth logic gate coupled to the array, an enable input and an output of the first gate, for detecting a first over-programmed condition, a fifth logic gate coupled to the array, an enable input and an output of the second logic gate, for detecting a second over-programmed condition and a sixth logic gate coupled to the array, an enable input and an output of the third logic gate, for detecting a third over-programmed condition as recited in claim 6. Applicant respectfully requests the withdrawal of the rejection, and reconsideration and allowance of claim 6.

Claims 7 and 8 depend, either directly or indirectly, on independent claim 3 and are believed to be in condition for allowance at least for the reasons provided with respect to independent claim 6.

Claims 9-12

For the reasons provided above, Applicant is unable to find, among other things, in the cited portions of Endoh, a multistate memory system comprising at least one over-programming condition detector, wherein the over-programming condition detector comprises a first logic gate for detecting a first one of the at least four sequential data states, a second logic gate for detecting a second one of the at least four sequential data states, a third logic gate for detecting a third one of the at least four sequential data states, a fourth logic gate coupled to the buffer and over-programming detection logic connected to the first, second, third and fourth logic gates for

generating an over-programming condition signal as recited in claim 9. Applicant respectfully requests the withdrawal of the rejection, and reconsideration and allowance of claim 9.

Claims 10-12 depend, either directly or indirectly, on independent claim 9 and are believed to be in condition for allowance at least for the reasons provided with respect to independent claim 9.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 371-2138 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

SCHWEGMAN, LUNDBERG & WOESSNER, P.A.
P.O. Box 2938
Minneapolis, MN 55402
(612) 373-6960

Date 5/13/2008

By Paul D. Kegley
Paul G. Kegley
Reg. No. 60,336

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being filed using the USPTO's electronic filing system EFS-Web, and is addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on this 13th day of May 2008.

Leshere Wolfe — Leshere Wolfe

Name — Signature